

## **ABSTRACT**

The present application is a protocol for maintaining cache coherency in a CMP. The CMP design contains multiple processor cores with each core having its own private cache. In addition, the CMP has a single on-chip shared cache. The processor cores and the shared cache may be connected together with a synchronous, unbuffered bidirectional ring interconnect. In the present protocol, a single INVALIDATEANDACKNOWLEDGE message is sent on the ring to invalidate a particular core and acknowledge a particular core.